

M

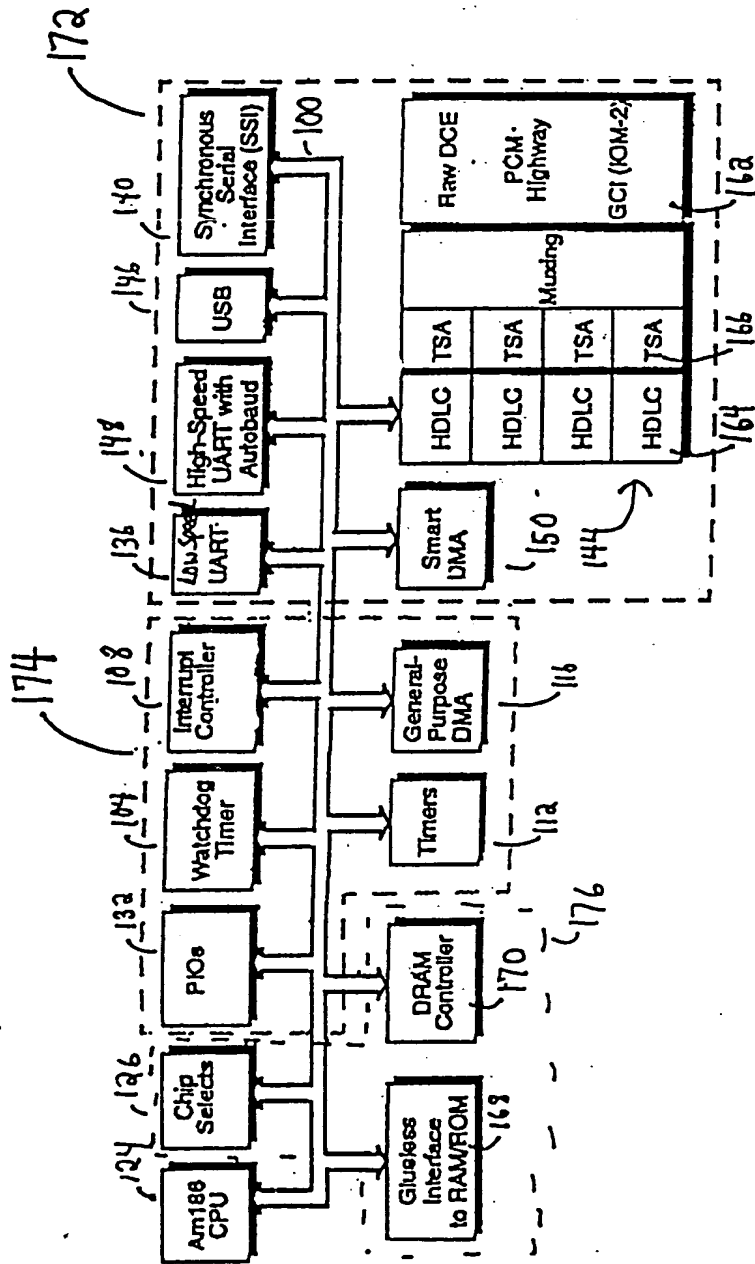
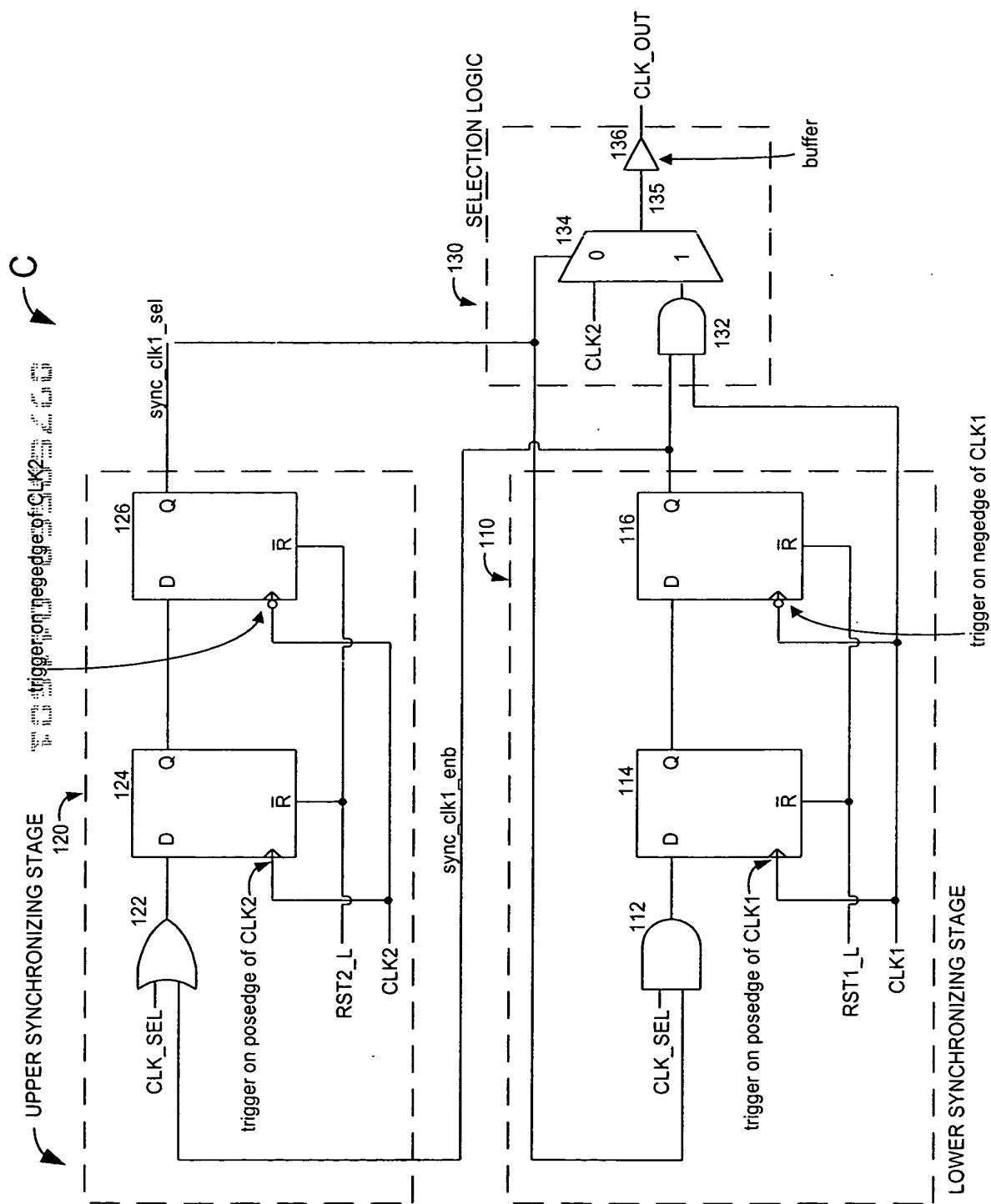


Fig. 1



**Notes:**

- \* RST2\_L is system reset synchronized to CLK2.
- \* RST1\_L is system reset synchronized to CLK1.
- \* CLK\_SEL is an asynchronous signal.

Figure 2a

# Synthesized (gate implementation) schematic from Verilog RTL

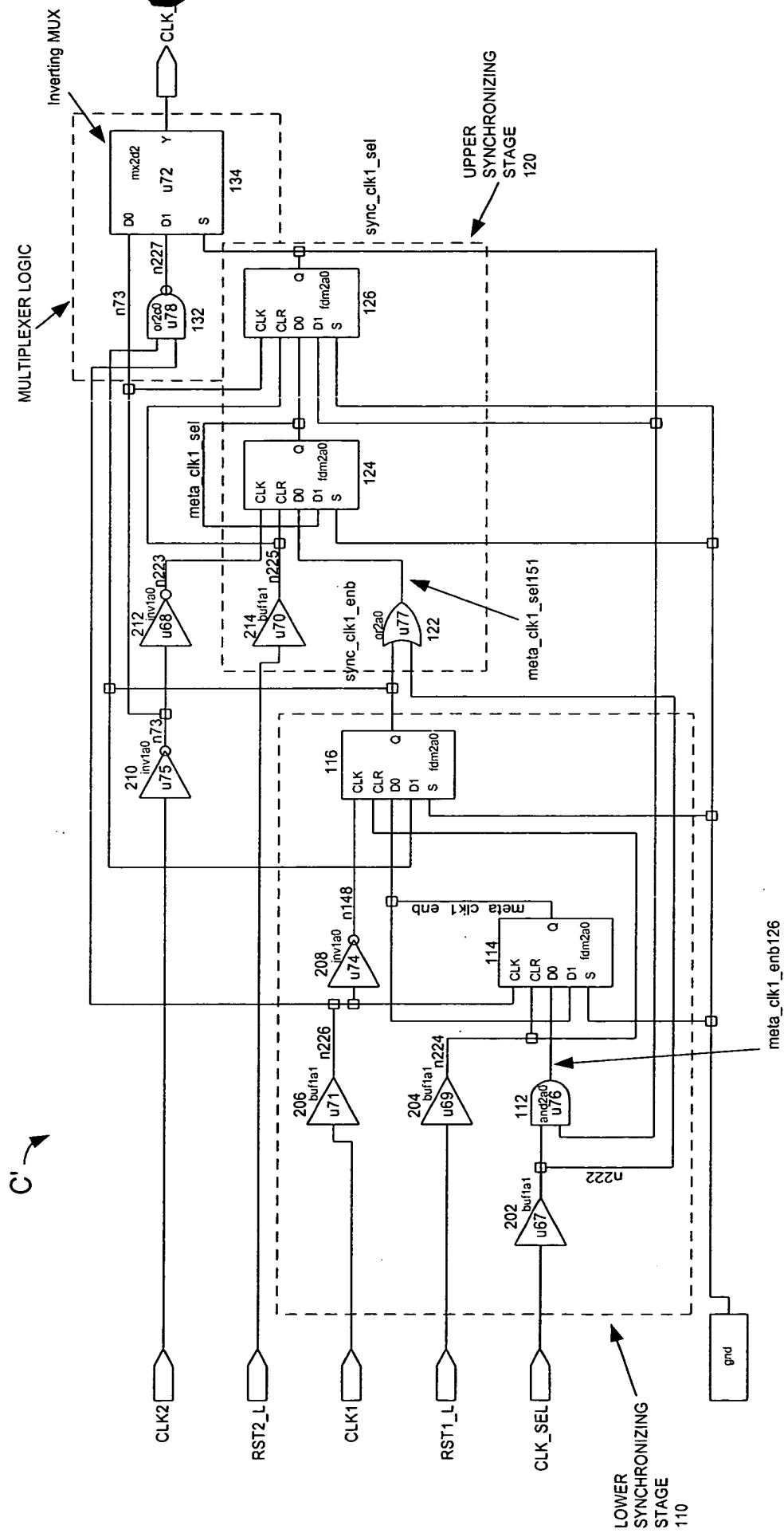
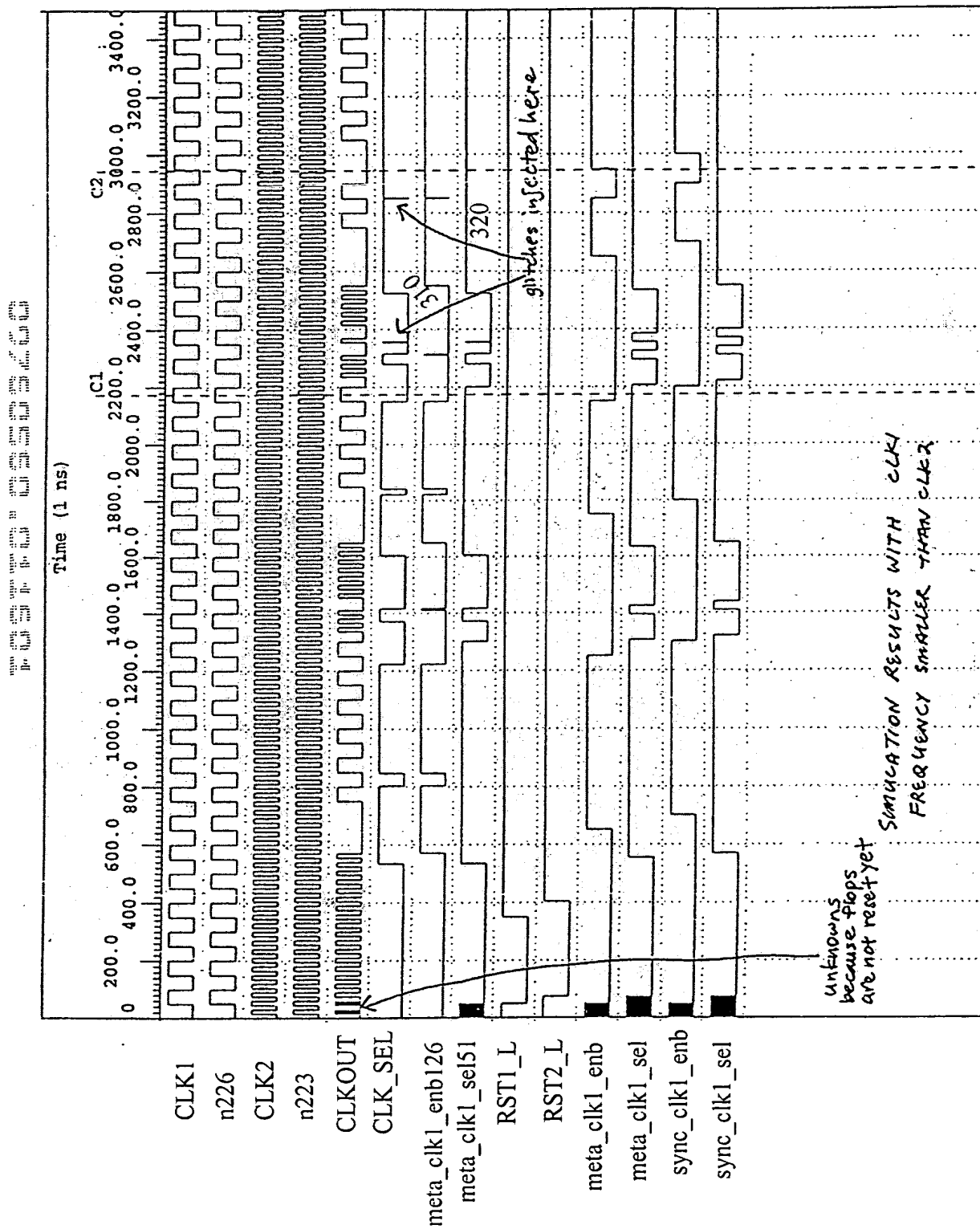


Figure 2b





### Figure 3

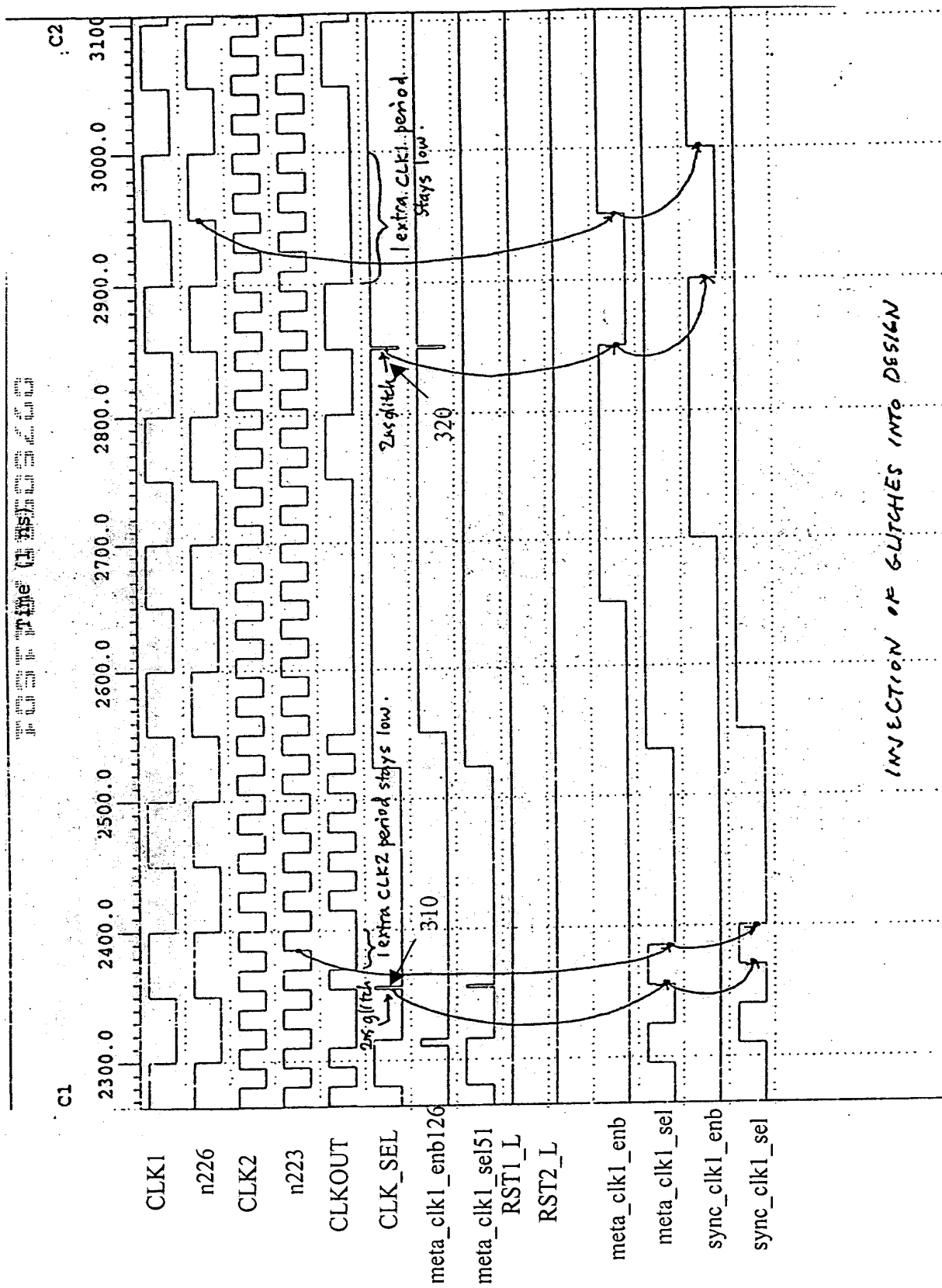


Figure 4

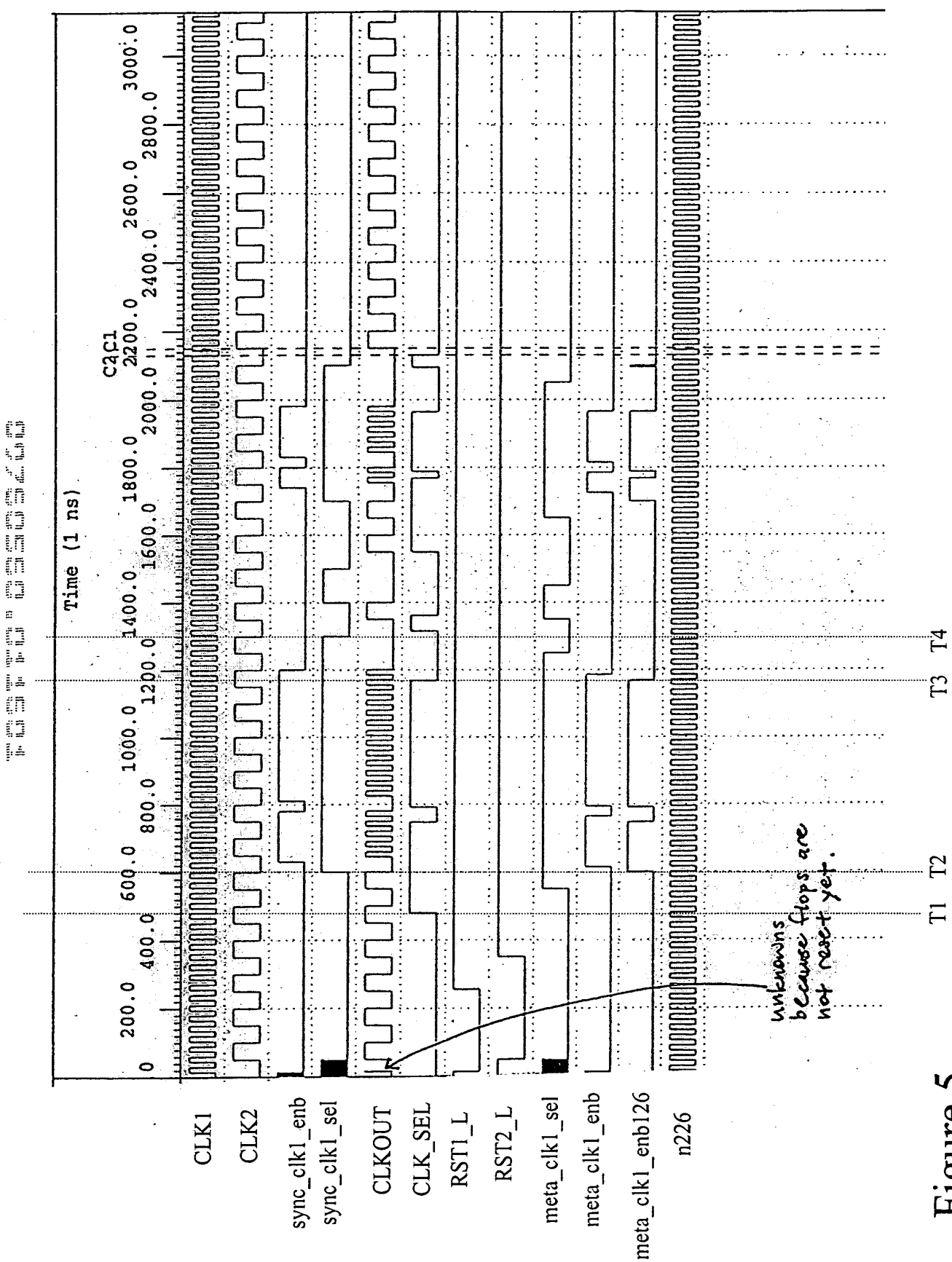


Figure 5